International Journal of Scientific & Engineering Research, Volume 6, Issue 7, July-2015
ISSN 2229-5518

Conversion of Synchronous HDL to Asynchronous Layout using industry standard Synchronous EDA tools

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***Abstract*— Synchronous circuits are widely used in existing systems. The most significant problem with these synchronous systems is clock skew. The clock skew is insignificant for smaller circuits. But as circuits become complex, this difference becomes very significant and extra design time and often extra circuitry needs to be used to solve the problem. With problems caused by the clock, it is very tempting to simply remove it from the system. This is the fundamental idea behind asynchronous system design. The proposed method describes the techniques to design Asynchronous (clock less) digital system. It is not as simple as just removing the clock, since the operation of the circuit must still be controlled by some other methods. Asynchronous circuits essentially govern themselves. The proposed asynchronous system design is based on Null Convention Logic (NCL) and handshaking protocol. The proposed methodology is to convert a Synchronous HDL to an Asynchronous Layout using industry standard synchronous EDA tools.**

Keywords*— *Asynchronous Systems; Null Convention Logic(NCL);EDA tools

I. INTRODUCTION

The invention of Integrated Circuits (IC's), explored the world of high efficient, less power electronic devices, in lesser area. Area, Power, Speed are the main constraints while designing a system. There should be proper trade-offs between these three constraints. Now a day, IC's are used in wide variety of applications, like commercial, industrial, space, military etc. The working environment of these applications will be with high temperature, pressure, radiation etc. The design of microelectronic devices in this type of working environment is a challenging task [1].

According to Moore's law, it is estimated that by 2016, the feature size will become 10 nm and the clock speed get increased to 28.7 GHz [2]. As the number of transistors in unit area decreases and clock speed increases, it is difficult to distribute clock properly to all modules. The problem of clock skew get dominates [7]. The other problems arise with clock are electromagnetic noise, power dissipation, worst case delay, problem with reusable modules [3].The idea of asynchronous system is not a new one [8]. It is there from 1950's. Recently, asynchronous systems are taking more attention. According to International Technology Roadmap for Semiconductors (ITRS) reports, asynchronous system will become majority share of the today's electronic devices by 2016. They also report that asynchronous system can overcome the problems of synchronous circuits [4][9].

This paper tries to implement an asynchronous system methodology using Null Convention Logic (NCL) and handshaking methods. The proposed methodology converts a synchronous HDL code to an Asynchronous Layout using industry standard synchronous EDA tools.

II. ASYNCHRONOUS CIRCUITS

Synchronous and Asynchronous systems are the two major classifications of digital systems. The Synchronous systems are based on the assumption that all signals are binary and discrete in time. These systems work with the help of global clock [5]. The figure 1 shows a Synchronous system. Functional blocks are represented by FB1 and FB2. Registers are used to store the data values. Here Reg 1, Reg 2 and Reg 3 are used for that. In synchronous system, the arrival of clock triggers the computation. Set up and Hold are the main two criteria for proper data propagation [5].

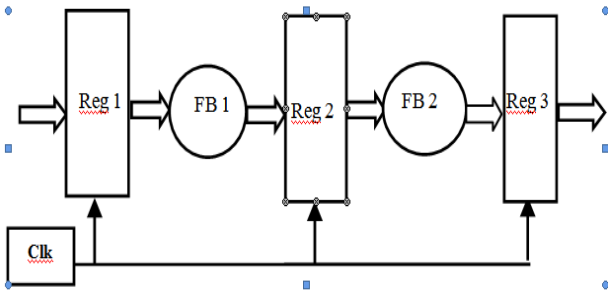

Fig. 1. Synchronous System

Asynchronous circuits are based on the assumptions that signals are binary and time is not discrete. Asynchronous circuits avoid the global clock. Here the data availability triggers the computation. Based on the logic style, asynchronous systems are classified into Delay Insensitive (DI) logic and Bounded Delay logic [3]. DI logic is shown in the figure 2.

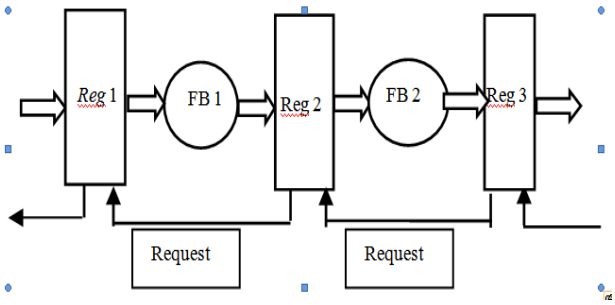

Fig. 2. Delay Insensitive Logic

DI uses handshaking protocols to achieve control over the circuit. A request signal is sent to previous functional modules requesting a new data after finishing its current operation. The previous block transfer the new data after receiving the request signal if it has completed its current operation. Otherwise the data will be hold. The delay insensitive circuits are insensitive to propagation delay of gates and wires.

Bounded delay model consist of delay lines. The propagation delay of the delay lines should be greater than the propagation delay of the functional block. The Bounded Delay asynchronous logic is shown in the figure 3.

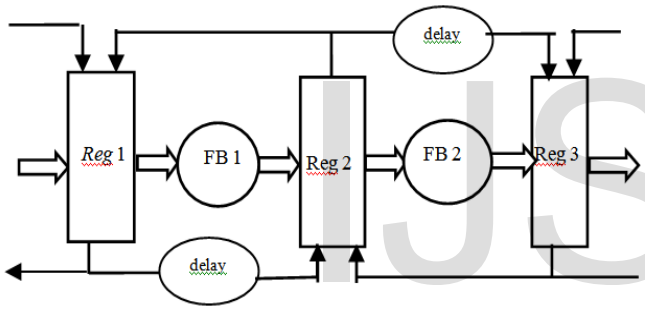

Fig. 3. Bounded Delay Model

III. NULL CONVENTION LOGIC

The delay insensitive circuits are implemented by using Null Conventional Logic (NCL) [10]. NCL is symbolically complete logic [6]. A symbolically complete expression means an expression which is complete in terms of relationship between the variables present in that expression. Traditional Boolean logic is not symbolically complete. Traditional Boolean logic can be made symbolically complete by two steps. First, assign a new value to show the validity and invalidity of data. In NCL, NULL is used for that. Second, enforce the criteria of completeness among the NULL and data value. NCL achieves delay insensitiveness by its coding. The dual rail encoding is the simplest one. The Table 1 shows the dual rail encoding of the values.

The major two criteria for NCL are Input Completeness and Observability [7]. The input completeness means, output should only change from NULL to data after all the input get changed from NULL to data. The Observability means, there should be no orphan propagation through gates. Each input and output should observable.

TABLE I. DUAL RAIL ENCODING

WAVEFRONT	True Value	False Value
DATA 1	1	0
DATA 0	0	1
NULL	0	0
INVALID CONDITION	1	1

The state holding ability of NCL makes them capable of tolerating radiation hardened environment [8]. The element that is used by NCL to achieve state holding ability is the threshold gate .A threshold gate shown in the figure 4. Threshold gate is represented by THmn. It implies that the output should be asserted only when m out of n inputs are asserted. The holding capability of a state can be achieved by two methods. They are Feedback solution methods and Intermediate solution methods [6]. Figure 4.1 shows TH22 gate. Figure 4.2 shows its simulated output. The state holding ability can be observed from the figure.

Fig. 4. Threshold Gate

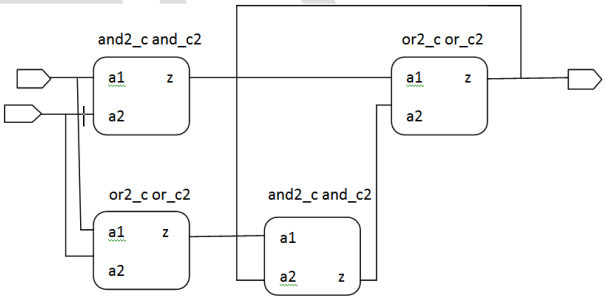

Fig. 4.1. RTL of TH22 Gate

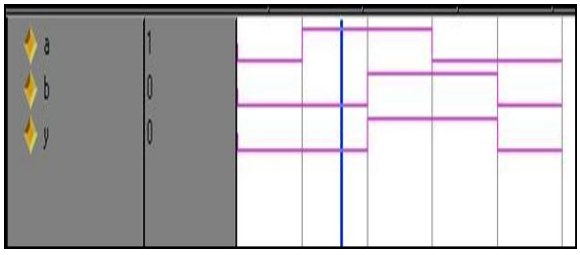

Fig. 4.2. Simulated Output of TH22 Gate

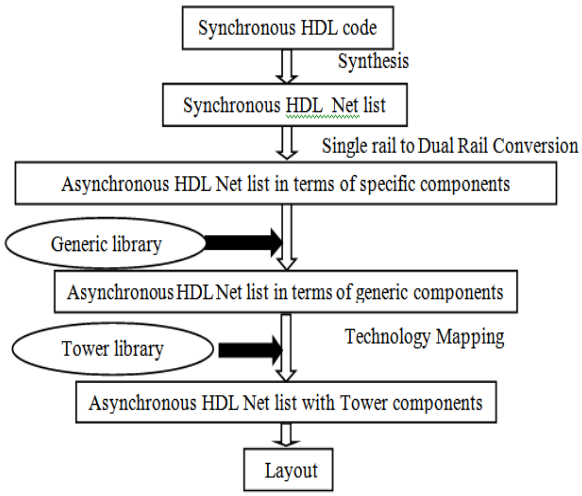

Fig. 5. Proposed Methodology

The proposed methodology for Asynchronous System Design is shown in the figure 5. This methodology defines the path from a Synchronous RTL code to an Asynchronous layout. The work is done with the help of tower library, tsl18fs120 pdk

IV. DESIGN OF A TWO BIT COUNTER

A two bit counter counts as 00,01,10,11. This is a synchronous counter works with the help of a clock.

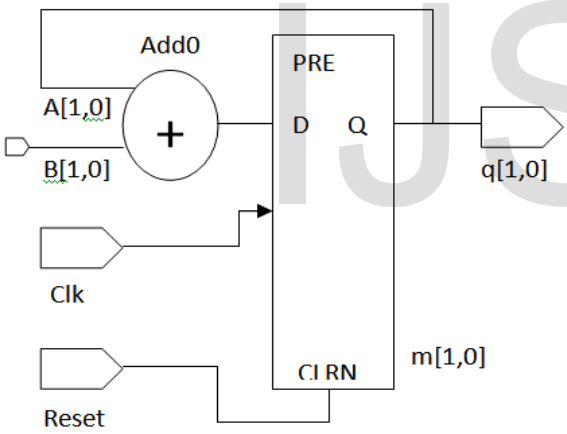

Fig 7. RTL of Synchronous 2-bit Counter

The net list is obtained after logic synthesis. The basic components used are two D flip-flops, an XOR, an Inverter. The figure of structural view of two bit counter is shown in the figure 7.1.

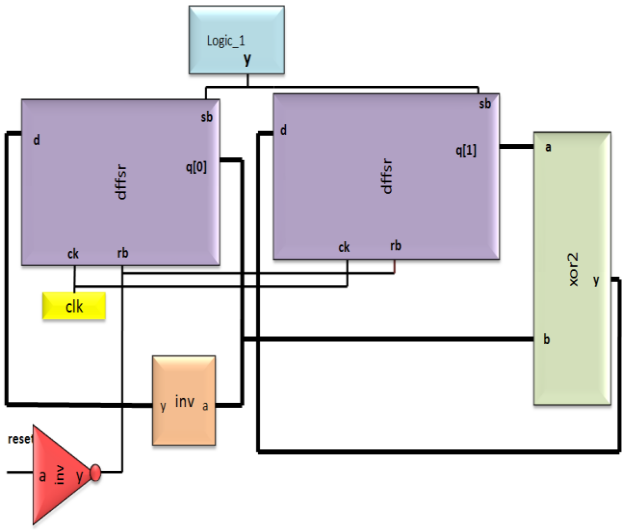

Fig. 7.1. RTL of Synchronous Single Rail 2-bit Counter

The next step is converting this to an asynchronous HDL net list. This involves mainly five steps. Dual rail expansion, Inverter removal, Mapping to threshold gate and asynchronous latches, Acknowledgement generation, Half latch implementation. The RTL after dual rail expansion is shown in the figure 7.2. Inputs and outputs are spilt into its true and false value.

The RTL after inverter removal is shown in the figure 7.3. Interchanging of true and false value will avoid an inverter. The figure 7.4 shows an RTL after mapping to threshold gates. An XOR gate is converted two th24comp gates.

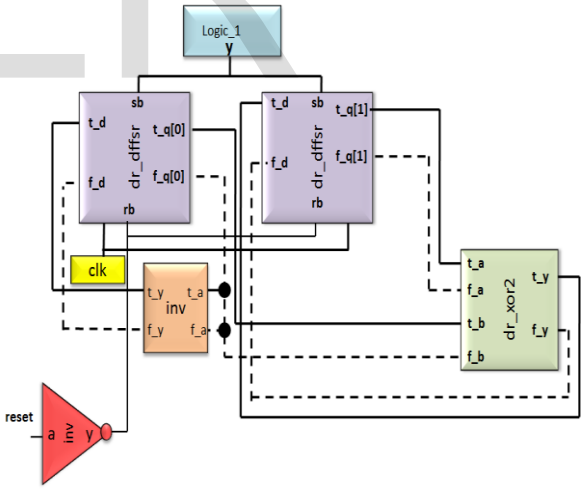

Fig. 7.2. RTL of Dual Rail Expanded 2-bit Counter

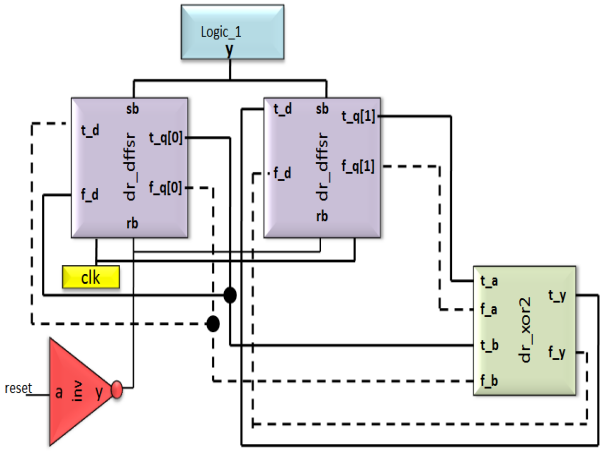

Fig. 7.3. RTL of 2-bit Counter after Inverter Removal

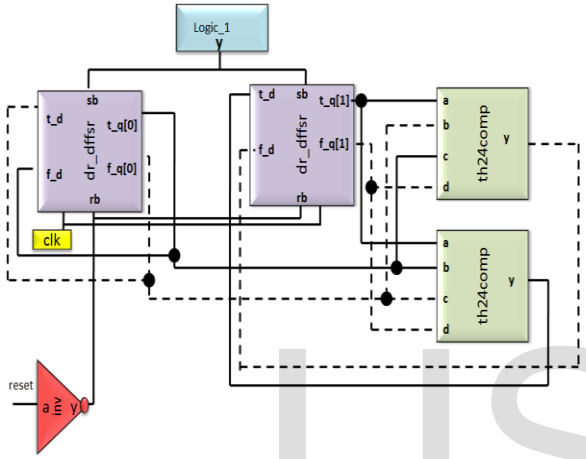

Fig. 7.4. RTL of 2-bit Counter after Mapping to threshold gate

The next step is Acknowledgement generation. There is ACKIN and ACKOUT. This is a complete implementation of NCL. Also the latches get changed to asynchronous latches. In this stage, number of signals is very few because the D flip-flops are not yet been flattened to three half latch implementations. Acknowledgement generation is shown in the figure 7.5.

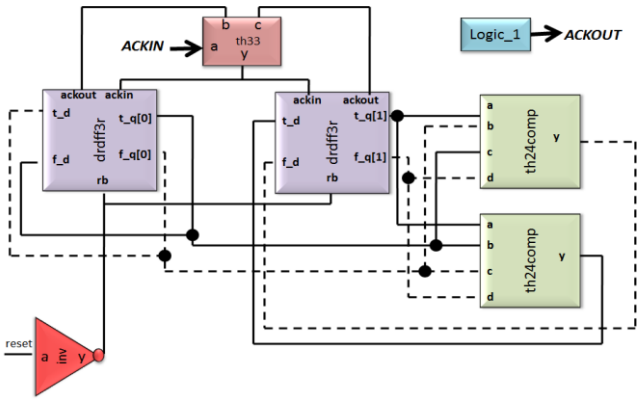

Fig. 7.5. RTL of 2-bit Counter after Acknowledgment Generation

The last step is half latch implementation. Here, the D flip-flops are flatted into three latches. Half latch implementation is for proper wave front propagation. This is shown in the figure 7.6.

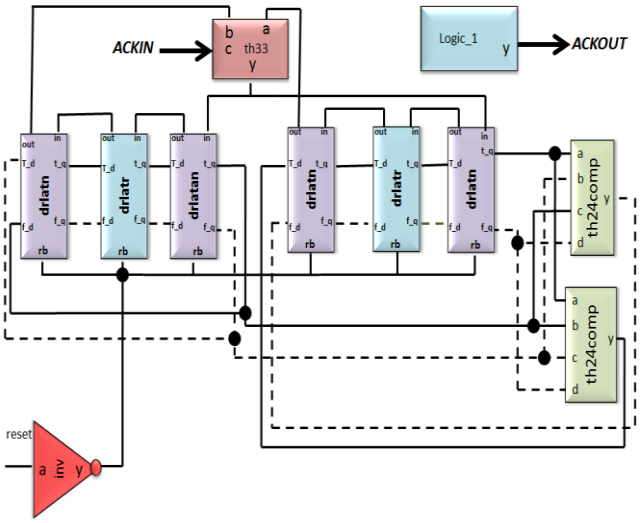

Fig. 7.6. RTL of NCL 2-bit Counter after mapping to Half Latchs

The simulation result of synchronous and asynchronous counter is shown in the figure 8 and figure 9 respectively.

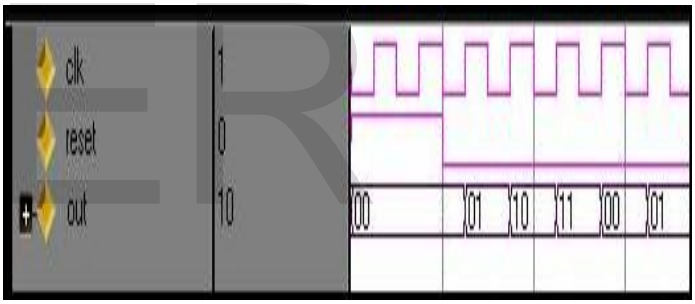

Fig. 8. Simulated Output of 2-BIT Synchronous Counter

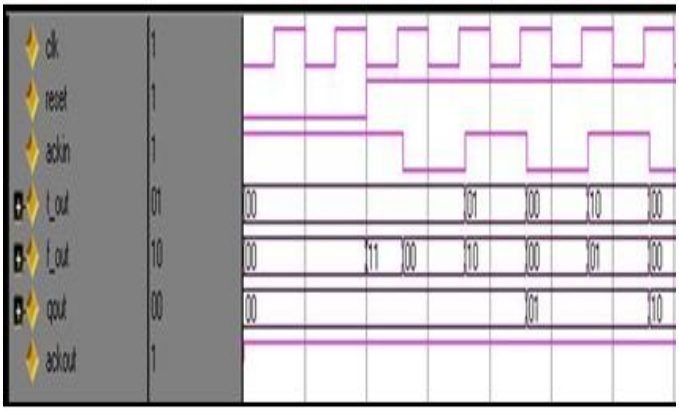

Fig. 9. Simulated Output of 2-BIT Asynchronous Counter

V. PHYSICAL DESIGN OF SYNCHRONOUS TWO BIT COUNTER

For performing physical design, Synopsis IC Compiler is used. It is a Place and route tool. After providing required library files, we import our design on to IC Compiler. As soon as design (.ddc file of Synchronous ALU) is imported, design view is generated. Next step is to create floorplan. Floor plan information includes the core area, top-level ports, and placement sites

Next step is to create power straps and rings into the design. After that placement is done. In this step, standard cells for the design are automatically placed in horizontal placement rows.

Next step is the clock tree synthesis. In this step, clock trees are build in such a way that it meets all the design rule constraints that minimizes the clock skew. Next is the routing step. Routing and routing optimization is performed here. Figure 10 show the design after routing was performed. This is the layout of synchronous counter.

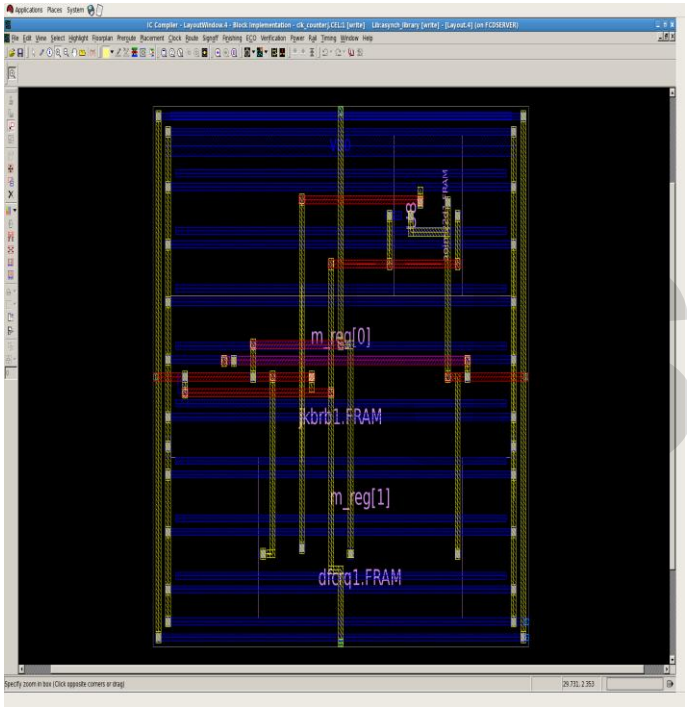

Fig. 10. Layout of a 2-BIT Synchronous Counter

VI. PHYSICAL DESIGN OF ASYNCHRONOUS TWO BIT COUNTER

Synopsys IC Compiler was used to design Asynchronous counter. First step in asynchronous method consists of developing the design views and layouts for the components which are in the design. After that layout is created by implementing various steps such as place and routing, floor planning, creating power straps placement and finally routing. Figure 11 shows the layout of an asynchronous counter.

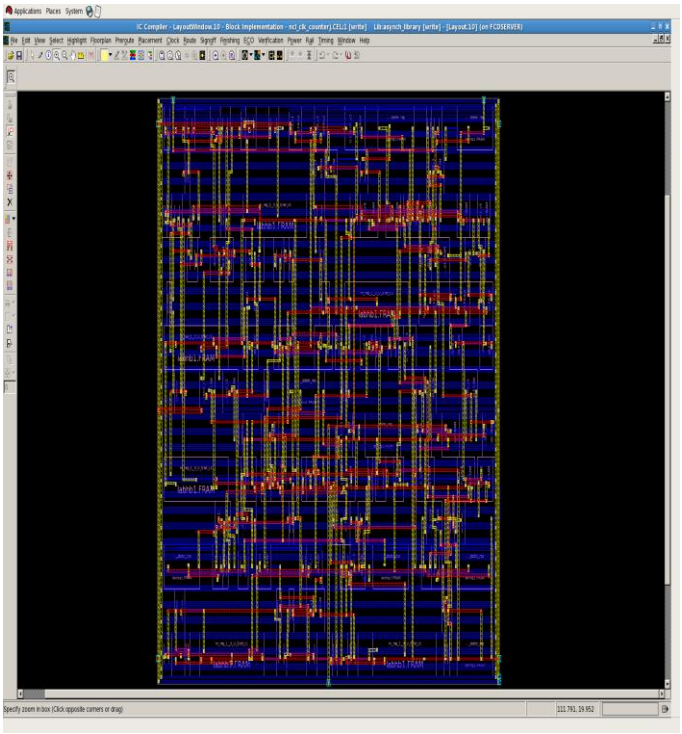

Fig. 11. Layout of a 2-BIT Asynchronous Counter

VII. CONCLUSION

In the present scenario, Asynchronous digital systems have more advantages over the Synchronous digital systems. The parameters such as EMI, skew problems, power consumption etc. are reduced in the clock-less system but they suffer from hazards and power consumption by the internal sub system of the clock-less digital system and also the design complexity is high. The proposed clock-less system overcomes the problems associated with the various radiation effects in space. The design of new methodology in asynchronous system overcome the effects of glitches, validity of the data, delay problems, hazards etc. But the major problem associated with asynchronous design is lack of CAD tools.

Here a methodology is developed for creating a path from Synchronous RTL code to Asynchronous Layout. The methodology is proved by designing a two bit counter. It has been observed that the area requirement is more in asynchronous design when comparing with synchronous design.

However, the lack of tools to design asynchronous circuits is a fundamental issue. We can see that, not only university laboratories but also industrial laboratories are seriously investigating the field of asynchronous VLSI design. We believe that asynchronous circuits will be a commercial reality in the next few years.

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